

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Amaresh Pangal et al.

Examiner: Unknown

Serial No.: Unknown

Group Art Unit: Unknown

Filed: Herewith

Docket: 884.400US1

Title: FLOATING POINT MULTIPLY ACCUMULATOR

J1017 U.S. PTO
09/873557
06/04/01

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

#2
C. B. Reed
9-3-01

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. § 1.97(b)(3), it is believed that no fee or certificate is required with this Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

AMARESH PANGAL ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 371-2159

Date

6-4-01

By

Dana B. LeMoine

Dana B. LeMoine
Reg. No. 40,062

"Express Mail" mailing label number: EL806497435US

Date of Deposit: June 4, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Form 1449*	Atty. Docket No.: 884.400US1	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Amaresh Pangal et al.	
	Filing Date: Herewith	Group: Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	5,764,089	06/09/1998	Partovi, H., et al.	327	200	08/30/96
	5,898,330	04/27/1999	Klass, E.F.	327	210	06/03/97
	5,900,759	05/04/1999	Tam, K.W.	327	201	06/26/97

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
-----------------------	-----------------	------	---------	-------	----------	-----------------------

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	Beaumont-Smith, A., et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", <u>Proceedings of the 14th IEEE Symposium on Computer Arithmetic</u> , 8 pgs., (1998)
	Even, G., et al., "On the Design of IEEE Compliant Floating Point Units", <u>IEEE Transactions on Computers</u> , Vol. 49, 398-413, (May 2000)
	Goto, G., et al., "A 54 X 54-b Regularly Structured Tree Multiplier", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 27, 1229-1236, (Sept. 1992)
	Ide, N., et al., "2.44-GFLOPS 300-MHz Floating-Point Vector-Processing Unit for High-Performance 3-D Graphics Computing", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 35, 1025-1033, (July 2000)
	Klass, F., "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic", <u>Proceedings of the Symposium on VLSI Circuits, Digest of Technical Papers</u> , Honolulu, HI, IEEE Circuits Soc. Japan Soc. Appl. Phys. Inst. Electron., Inf. & Commun. Eng. Japan, pp. 108-9, (1998)
	Lee, K.T., et al., "1 GHz Leading Zero Anticipator Using Independent Sign-Bit Determination Logic", <u>2000 Symposium on VLSI Circuits Digest of Technical Papers</u> , 194-195, (2000)
	Partovi, H., et al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements", <u>Proceedings of the IEEE International Solid-State Circuits Conference, Digest of Technical Papers and Slide Supplement</u> , NexGen Inc., Milpitas, CA, 40 pgs., (1996)

Examiner

Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.